MULTIPHASE CLOCK GENERATORS

TECHNICAL FIELD OF THE INVENTION

[0001] The present invention relates generally to clock generators and in particular the present invention relates to multiphase clock generators.

BACKGROUND OF THE INVENTION

[0002] Clock signals are used for timing or synchronizing operations within many electronic devices. For example, clock signals are used for timing or synchronizing read and write operations for memories, such as flash memories, dynamic random access memories (DRAMs), static random access memories (SRAMs), etc., of electronic devices, such as desktop or portable computers. For some applications, clock signals are used to control data latching for read and write applications. For one application, such as for double-data-rate DRAMs, it is advantageous to latch data, for example, every half-clock cycle. This typically involves using a first latch of a latch system to latch data when the clock signal goes from low to high, i.e., on a positive clock transition (or positive clock edge), and using a second latch of the latch system to latch data a half clock cycle later when the clock signal goes from high to low, i.e., on a negative clock transition (or negative clock edge).

[0003] Typically, latches that latch data on positive clock transitions are of a different type than latches that latch data on negative clock transitions. For example, latches that latch data on positive clock transitions are often p-channel devices, whereas latches that latch data on negative clock transitions are often n-channel devices. One problem with this is that different type latches can cause timing variations that can distort the data output of the latch system. Therefore, it is often advantageous to latch data on a single clock edge, either positive or negative. Four-phase clocks can used to generate positive or negative clock edges at half clock cycle intervals. Each clock phase is then used to control a latch of a latch system having common latch types.

[0004] One method of developing a four-phase clock is to use each phase of a two phase-clock to drive two clock dividers. The clock dividers are then started in sequence at

half clock cycle intervals. This often involves aligning a first phase of the two-phase clock with a second phase of the two-phase clock so that the first and second phases are a half clock cycle out of phase. That is, so that the first clock phase transitions high when the second clock phase transitions low and vice versa. Then, a first divider is started from a reset state when the first phase of the two-phase clock transitions high to start the first phase of the four-phase clock. A half clock cycle later, a second divider is started from a reset state when the second phase of the two-phase clock transitions high to start the second phase of the four-phase clock. Another half clock cycle later, a third divider is started from a reset state when the first phase of the two-phase clock transitions high again to start the third phase of the four-phase clock. Another half-clock cycle later, a fourth divider is started from a reset state when the second phase of the two-phase clock transitions high again to start the fourth phase of the four-phase clock. However, for relatively high frequencies, the half cycle intervals do not provide enough time to start the dividers owing to logic delays and startup times for the dividers.

[0005] For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for alternatives for starting phases of multiphase clocks.

SUMMARY

[0006] The above-mentioned problems with clock generators and other problems are addressed by the present invention and will be understood by reading and studying the following specification.

[0007] Various embodiments of the present invention relate to multiphase clock generators and methods. The clock generators generate multiple clock phases from one or more input clock signals using clock dividers. Successive clock phases are started out of order to provide more time between starting the clock phases for starting the clock dividers. After all of the clock phases are started, the clock phases are aligned so that successive clock phases are evenly displaced.

[0008] For one embodiment, the invention provides a multiphase clock generator with a first clock divider for generating a first-phase clock signal from a first input clock signal. A first logic gate is connected to an output port of the first clock divider. A second clock divider is connected to an output port of the first logic gate. The second clock divider is for generating a second-phase clock signal from the first input clock signal. A second logic gate is connected to an output port of the second clock divider. A third clock divider is connected to an output port of the second logic gate. The third clock divider is for generating a third-phase clock signal from a second input clock signal.

[0009] For another embodiment, the invention provides a memory device having an array of memory cells and control circuitry for controlling access to the array of memory cells. The control circuitry has a multiphase clock generator. The multiphase clock generator has a first clock divider for generating a first-phase clock signal from a first input clock signal. An input port of the first clock divider is connected to a first inverter. A first logic gate is connected to an output port of the first clock divider. A second clock divider is connected to an output port of the first logic gate through a second inverter. The second clock divider is for generating a second-phase clock signal from the first input clock signal. A second logic gate is connected to an output port of the second clock divider. A third clock divider is connected to an output port of the second logic gate through a third inverter. The third clock divider is for generating a third-phase clock signal from a second input clock signal. A third logic gate is connected to an output port of the third clock divider. A fourth clock divider is connected to an output port of the third logic gate through a fourth inverter. The fourth clock divider is for generating a fourth-phase clock signal from the second input clock signal.

[0010] For another embodiment, the invention provides a method of operating a multiphase clock generator. The method includes starting a first-phase clock signal at a first clock edge of a first input clock signal. At least one clock cycle of the first input clock signal after starting the first-phase clock signal, the method includes starting a second-phase clock signal at a second clock edge of the first input clock signal. After starting the second-phase clock signal, the method includes starting a third-phase clock signal at a first

clock edge of a second input clock signal so that a clock edge of the third-phase clock signal occurs a half a clock cycle of the first input clock signal after a clock edge of the first-phase clock signal and the half the clock cycle of the first input clock signal before a clock edge of the second-phase clock signal. The first and second input clock signals have the same frequency and are half the clock cycle of the first input clock signal out of phase. The clock edges of the first-, second- and third-phase clock signals are like clock edges. At least one clock cycle of the first input clock signal after starting the third-phase clock signal, the method includes starting a fourth-phase clock signal at a second clock edge of the second input clock signal so that a clock edge of the fourth-phase clock signal occurs the half the clock cycle of the first input clock signal after the clock edge of the second-phase clock signal, wherein the clock edges of the second- and fourth-phase clock signals are like clock edges.

[0011] Further embodiments of the invention include methods and apparatus of varying scope.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] Figure 1 illustrates a multiphase clock generator according to an embodiment of the present invention.

[0013] Figure 2 illustrates timing of various clock phases according to another embodiment of the present invention.

[0014] Figure 3 is a block diagram of a memory system according to another embodiment of the present invention.

DETAILED DESCRIPTION

[0015] In the following detailed description of the invention, reference is made to the accompanying drawings that form a part hereof, and in which is shown, by way of illustration, specific embodiments in which the invention may be practiced. In the drawings, like numerals describe substantially similar components throughout the several views. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, logical,

and electrical changes may be made without departing from the scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims and equivalents thereof.

[0016] Figure 1 illustrates a multiphase clock generator 100 according to an embodiment of the present invention. Clock generator 100 has clock dividers 102, 104, 106, and 108. For one embodiment, clock dividers 102 and 104 divide the frequency (or multiply the period) of an input clock signal CLK by a number, e.g., two, and clock dividers 106 and 108 divide the frequency (or multiply the period) of an input clock signal CLK_ by a number, e.g., two. CLK is received at input ports 112 and 114 respectively of clock dividers 102 and 104, while CLK_ is received at input ports 116 and 117 respectively of clock dividers 106 and 108.

[0017] For another embodiment, CLK and CLK_ are respective phases of a two-phase clock. CLK and CLK_ are illustrated in Figure 2. For one embodiment, CLK and CLK_ are complimentary clock cycles having the same period and are aligned so that they are a half clock cycle (or clock period) out of phase, i.e., 180 degrees, as shown in Figure 2. That is, positive clock edges 202 of CLK are shifted by a half-clock cycle from positive clock edges 206 of CLK_. This can be accomplished using a phase-locked loop (PLL), a delay-locked loop (DLL), etc. Positive clock edges 202 and 206 respectively correspond to CLK transitioning high (or going from low to high) and CLK_ transitioning high.

[0018] An inverter 118 is connected to an input port 120 of clock divider 102. Inverter 118 receives a reset signal R_, shown for one embodiment in Figure 2, and transmits a reset signal 119 that is an inversion of reset signal R_ to input port 120. An output port 122 of clock divider 102 is connected to an input port 124 of a logic gate 126, such as a Muller C gate. An inverter 130 is connected between an output 132 of logic gate 126 and an input port 134 of clock divider 104. Logic gate 126 also has an input port 136 for receiving reset signal R_.

[0019] It will be appreciated by those skilled in the art that the output of a Muller C gate goes to logical one (or high) if all inputs are logical one. The output goes to logical

zero (or low) if all inputs are logical zero. The output stays at the previous value if the inputs differ.

[0020] An output port 138 of clock divider 104 is connected to an input 140 of a logic gate 142, such as a modified (or asymmetric) Muller C gate. Logic gate 142 includes an input port 144 for receiving reset signal R_ and an input port 146 connected to a repeater (or buffer) 148 that for one embodiment, includes inverters 150 and 152. Repeater 148 receives CLK_ and sends CLK_ to input port 146 of logic gate 142 without changing the orientation of CLK_. For one embodiment, repeater 148 acts to decrease the load on CLK_. An inverter 154 is connected between an output port 156 of logic gate 142 and an input port 158 of clock divider 106.

[0021] It will be appreciated by those skilled in the art that the output of a modified Muller C gate goes to logic zero (or low) when first and second inputs are at logic zero, regardless of the logic value at a third input. The output goes to logic one (or high) when the second and third inputs are at logic one, regardless of the logic value at the first input. The output remains at the previous value for all other combinations of the logic values of the first, second, and third inputs.

[0022] An output port 160 of clock divider 106 is connected to an input port 162 of a logic gate 164, such as a Muller C gate. An inverter 166 is connected between an output 168 of logic gate 164 and an input port 170 of clock divider 108. Logic gate 164 also has an input port 172 for receiving reset signal R_. Clock divider 108 also has an output port 174. For another embodiment, output ports 122, 138, 160, 174 are connected to latches, such as read data latches, e.g., of a DRAM. For other embodiments, output ports 122, 138, 160, and 174 respectively output a phase-0 (PH0) clock signal, a phase-2 (PH2) clock signal, a phase-1 (PH1) clock signal, and a phase-3 (PH3) clock signal. The PH0, PH2, PH1, and PH3 clock signals are illustrated for one embodiment in Figure 2.

[0023] For one embodiment, when logic gate 126 (or logic gate 164) receives two inputs having a common logic value, an output of logic gate 126 (or logic gate 164) assumes the common logic value. When logic gate 126 (or logic gate 164) receives two inputs having different logic values, the output of logic gate 126 (or logic gate 164)

remains unchanged. For example, when both of the inputs of logic gate 126 (or logic gate 164) are logic ones (or logic highs), the output of logic gate 126 (or logic gate 164) is logic one (or logic high). When both of the inputs of logic gate 126 (or logic gate 164) are logic zeros (or logic lows), the output of logic gate 126 (or logic gate 164) is logic zero (or logic low). When the inputs of logic gate 126 (or logic gate 164) have different logic values, e.g., logic zero and logic one, the output of logic gate 126 (or logic gate 164) is the output from when both of the inputs previously had the same logic value. For example, when different logic input values follow two logic one inputs, the output stays at logic one, or when different logic input values follow two logic zero inputs, the output stays at logic zero.

[0024] For another embodiment, when the inputs to input ports 140 and 144 of logic gate 142 are both logic zeros (or logic low values), the output value at output port 156 is a logic zero (or a logic low value), regardless of whether the input to input port 146 is a logic one or zero (or a logic high or low value). When the inputs to input ports 140 and 146 are both logic ones (or logic high values), the output value at output port 156 is a logic one (or a logic high value), regardless of whether the input to input port 144 is a logic one or zero (or a logic high or low value). For all other combinations of input values to input ports 140, 144, and 146, the output value at output port 156 stays at the value from when the inputs to input ports 140 and 144 were last both logic zeros or when the inputs to input ports 140 and 146 were last both logic ones.

[0025] For one embodiment, reset signal R_ is initially low, as shown in Figure 2, and clock dividers 102, 104, 106, and 108 are initially at a reset state. When clock dividers 102, 104, 106, and 108 are at the reset state, the PH0, PH2, PH1, and PH3 clock signals are low, e.g., at a logic zero, as shown in Figure 2. For one embodiment, clock dividers 102, 104, 106, and 108 are in a reset state when reset signals 119, 180, 182, and 184 respectively at input ports 119, 134, 158, and 170 are high (or are turned on).

[0026] When reset signal R_ is low, reset signal 119 is high, causing signal divider 102 to be reset and thus the PH0 clock signal to be low. Consequently, the PH0 clock signal and reset signal R_ are respective low inputs of input ports 124 and 136 of logic gate 126,

causing the output of logic gate 126 to be low. Inverter 130 inverts the output of logic gate 126 to produce reset signal 180, thus reset signal 180 is high, clock divider 104 is at the reset state, and the PH2 clock signal is low. Consequently, the PH2 clock signal and reset signal R_ are respective low inputs of input ports 144 and 140 of logic gate 142, causing the output of logic gate 142 to be low. Inverter 154 inverts the output of logic gate 142 to produce reset signal 182, thus reset signal 182 is high, clock divider 106 is at the reset state, and the PH1 clock signal is low. Consequently, the PH1 clock signal and reset signal R_ are respective low inputs of input ports 162 and 172 of logic gate 164, causing the output of logic gate 164 to be low. Inverter 166 inverts the output of logic gate 164 to produce reset signal 184, thus reset signal 184 is high, clock divider 108 is at the reset state, and the PH3 clock signal is low.

[0027] When R_ transitions high, as shown in Figure 2, the reset signal 119 at input port 120 of clock divider 102 transitions low and is thus turned off, removing clock divider 102 from the reset state. When CLK transitions high, e.g., at a half a clock cycle of CLK after R_ transitions high, positive clock edge 202_2 of CLK is produced at input port 112 of clock divider 102. The PH0 clock signal starts at positive clock edge 202_2, e.g., by transitioning high to produce a positive clock edge 210_1 of the PH0 clock signal, as shown in Figure 2.

[0028] Consequently, the PH0 clock signal and reset signal R_ are respective high inputs of input ports 124 and 136 of logic gate 126, causing the output of logic gate 126 to be high and reset signal 180 to be low. Therefore, reset signal 180 is turned off and clock divider 104 is removed from the reset state. When positive clock edge 202_3 occurs at input port 114 of clock divider 104, the PH2 clock signal starts at positive clock edge 202_3, e.g., by transitioning high to produce a positive clock edge 220_1 of the PH2 clock signal, as shown in Figure 2.

[0029] For one embodiment, positive clock edge 220_1 coincides with negative clock edge 212 of the PH0 clock signal, as shown in Figure 2. That is, the PH0 clock signal transitions low when the PH2 clock signal transitions high and vice versa, and the PH0 and PH2 clock signals are one clock cycle of CLK out of phase. The one clock cycle of CLK

between the start of the PH0 and PH2 clock signals compensates for logic delays and startup times of the clock dividers that can cause problems at relatively high frequencies for conventional clock generators that generate successive clock phases at half cycle intervals of CLK.

[0030] The PH2 clock signal and reset signal R_ are respective high inputs of input ports 144 and 140 of logic gate 142. When CLK_ transitions high to produce positive clock edge 206_3 at input port 146 of logic gate 142 via repeater 148, the output of logic gate 142 goes high. Therefore, reset signal 182 is turned off and clock divider 106 is removed from the reset state. When positive clock edge 206_4 occurs at input port 116 of clock divider 106, the PH1 clock signal starts at positive clock edge 206_4, e.g., by transitioning high to produce a positive clock edge 230 of the PH1 clock signal, as shown in Figure 2.

[0031] For one embodiment, positive clock edge 206_4 occurs one-and-one-half clock cycles of CLK (or CKL_) after positive clock edge 202_3. This compensates for logic delays and startup times of the clock dividers. Moreover, the occurrence of positive clock edge 206_4 one-and-one-half clock cycles of CLK after positive clock edge 202_3 means that positive clock edge 230 occurs one-and-one-half clock cycles of CLK after positive clock edge 220_1 (the start) of the PH2 clock signal and thus one half clock cycle of CLK before a positive clock edge 220_2 of the PH2 clock signal occurs, as shown in Figure 2. Positive clock edge 206_4 occurs two-and-one-half clock cycles of CLK (or CKL_) after positive clock edge 202_2. This means that positive clock edge 230 occurs two-and-one-half clock cycles of CLK after positive clock edge 210_1 (the start) of the PH0 clock signal and thus one half clock cycle of CLK after a positive clock edge 210_2 of the PH0 clock signal occurs, as shown in Figure 2.

[0032] The PH1 clock signal and reset signal R_ are respective high inputs of input ports 162 and 172 of logic gate 164, causing the output of logic gate 164 to be high and reset signal 184 to be low. Therefore, reset signal 184 is turned off and clock divider 108 is removed from the reset state. When positive clock edge 206_5 of CLK_ occurs at input port 117 of clock divider 108, the PH3 clock signal starts at positive clock edge 206_5, e.g.,

by transitioning high to produce a positive clock edge 240 of the PH3 clock signal, as shown in Figure 2.

[0033] For one embodiment, positive clock edge 206_5 occurs one clock cycle of CLK (or CKL_) after positive clock edge 206_4. This compensates for logic delays and startup times of the clock dividers. Moreover, the occurrence of positive clock edge 206_5 one clock cycle of CLK after positive clock edge 206_4 means that positive clock edge 240 occurs one clock cycle of CLK after positive clock edge 230 (the start) of the PH1 clock signal and thus one half clock cycle of CLK after positive clock edge 220_2 of the PH2 clock signal and one-and-one-half clock cycles of CLK after positive clock edge 210_2 of the PH0, as shown in Figure 2. Therefore, positive clock edges 210_2, 230, 220_2, and 240, respectively of the PH0, PH1, PH2 and PH3 clock signals, are respectively displaced by one half of a clock cycle of CLK (or CKL_). This represents the proper displacement between the positive clock edges of the PH0, PH1, PH2, and PH3 clock signals for one embodiment. Note that this is accomplished by starting the PH0, PH1, PH2, and PH3 clock signals out of order, i.e., PH0, followed by PH2, followed by PH1, followed by PH3. Starting the PH0, PH1, PH2, and PH3 clock signals out of order provides more time for starting the clock dividers.

[0034] Figure 3 is a simplified block diagram of an integrated circuit memory device 300 as a dynamic memory device, e.g., a DRAM (Dynamic Random Access Memory), in accordance with an embodiment of the invention. The memory device 300 includes an array of memory cells 302, an address decoder 304, row access circuitry 306, column access circuitry 308, control circuitry 310 for controlling access to the array of memory cells 302, and Input/Output (I/O) circuitry 312.

[0035] The memory device 300 can be coupled to an external microprocessor 314, or memory controller for memory accessing as part of an electronic system. The memory device 300 receives control signals from the processor 314, such as WE*, RAS* and CAS* signals. The memory cells are used to store data that are accessed via I/O lines. Control circuitry 310 decodes the control signals from processor 314 and controls access to the memory cells. These signals are used to control the operations of memory device 300,

including data read and data write operations. The memory cells are accessed in response to the control signals and the address signals. For one embodiment, the control circuitry 310 includes circuitry for generating a multiphase clock, such as clock generator 100 of Figure 1, in accordance with the invention. It will be appreciated by those skilled in the art that additional circuitry and control signals can be provided, and that the memory device of Figure 3 has been simplified to help focus on the invention.

[0036] It will be understood that the above description of a DRAM is intended to provide a general understanding of the memory and is not a complete description of all the elements and features of a DRAM. Further, the invention is equally applicable to a variety of sizes and types of memory circuits known in the art, such as flash memory circuits, and is not intended to be limited to the DRAM described above.

CONCLUSION

[0037] Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement that is calculated to achieve the same purpose may be substituted for the specific embodiments shown. Many adaptations of the invention will be apparent to those of ordinary skill in the art. Accordingly, this application is intended to cover any adaptations or variations of the invention. It is manifestly intended that this invention be limited only by the following claims and equivalents thereof.